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STRUCTURE AND METHOD OF MAKING STRAINED CHANNEL CMOS TRANSISTORS HAVING LATTICE-MISMATCHED EPITAXIAL EXTENSION AND SOURCE AND DRAIN REGIONS

Abstract

A structure and method are provided in which an n-type field effect transistor (NFET) and a p-type field effect transistor (PFET) each have a channel region disposed in a single-crystal layer of a first semiconductor and a stress is applied at a first magnitude to a channel region of the PFET but not at that magnitude to the channel region of the NFET. The stress is applied by a layer of a second semiconductor which is lattice-mismatched to the first semiconductor. The layer of second semiconductor is formed over the source and drain regions and extensions of the PFET at a first distance from the channel region of the PFET and is formed over the source and drain regions of the NFET at a second, greater distance from the channel region of the NFET, or not formed at all in the NFET.